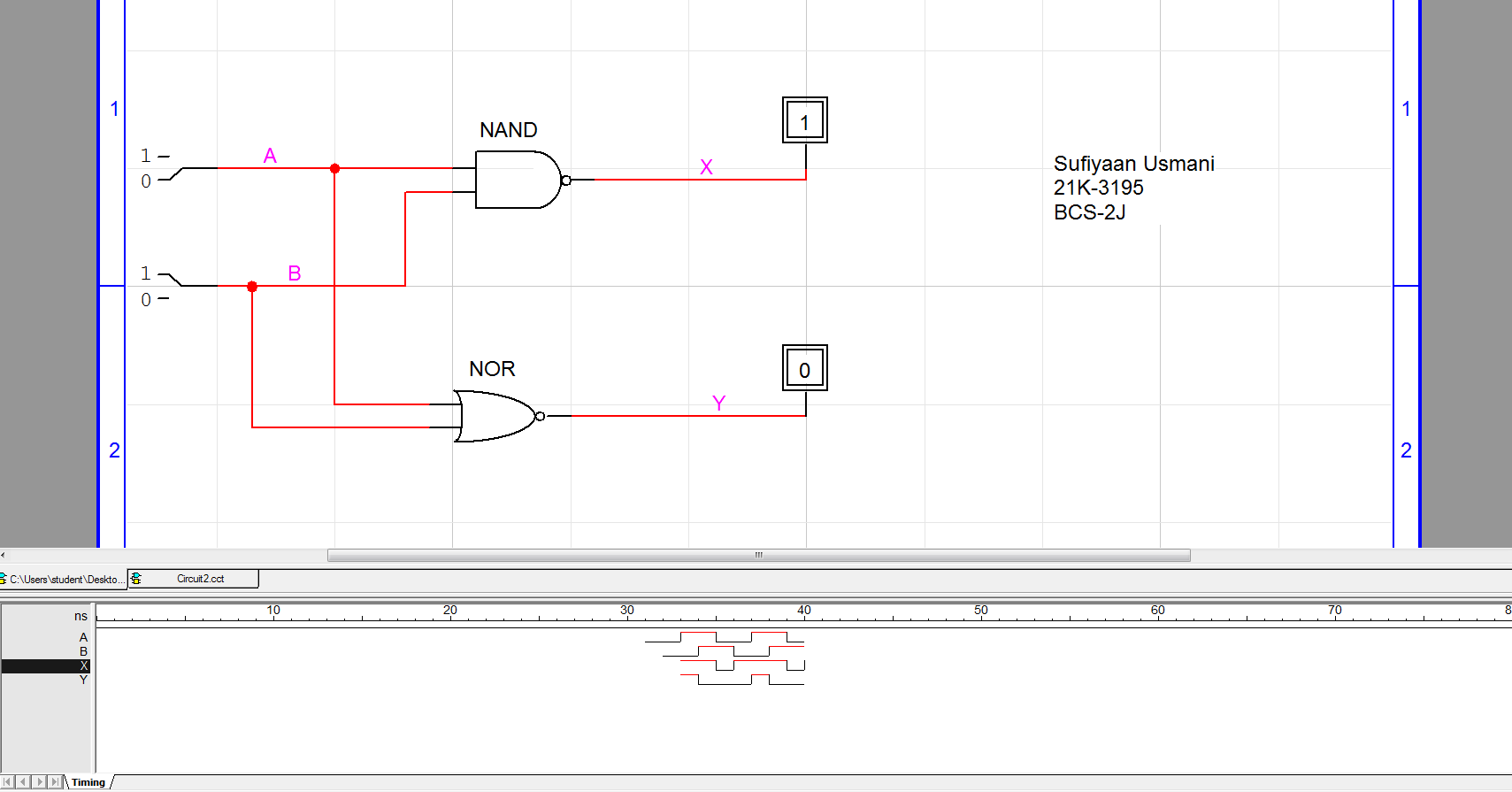
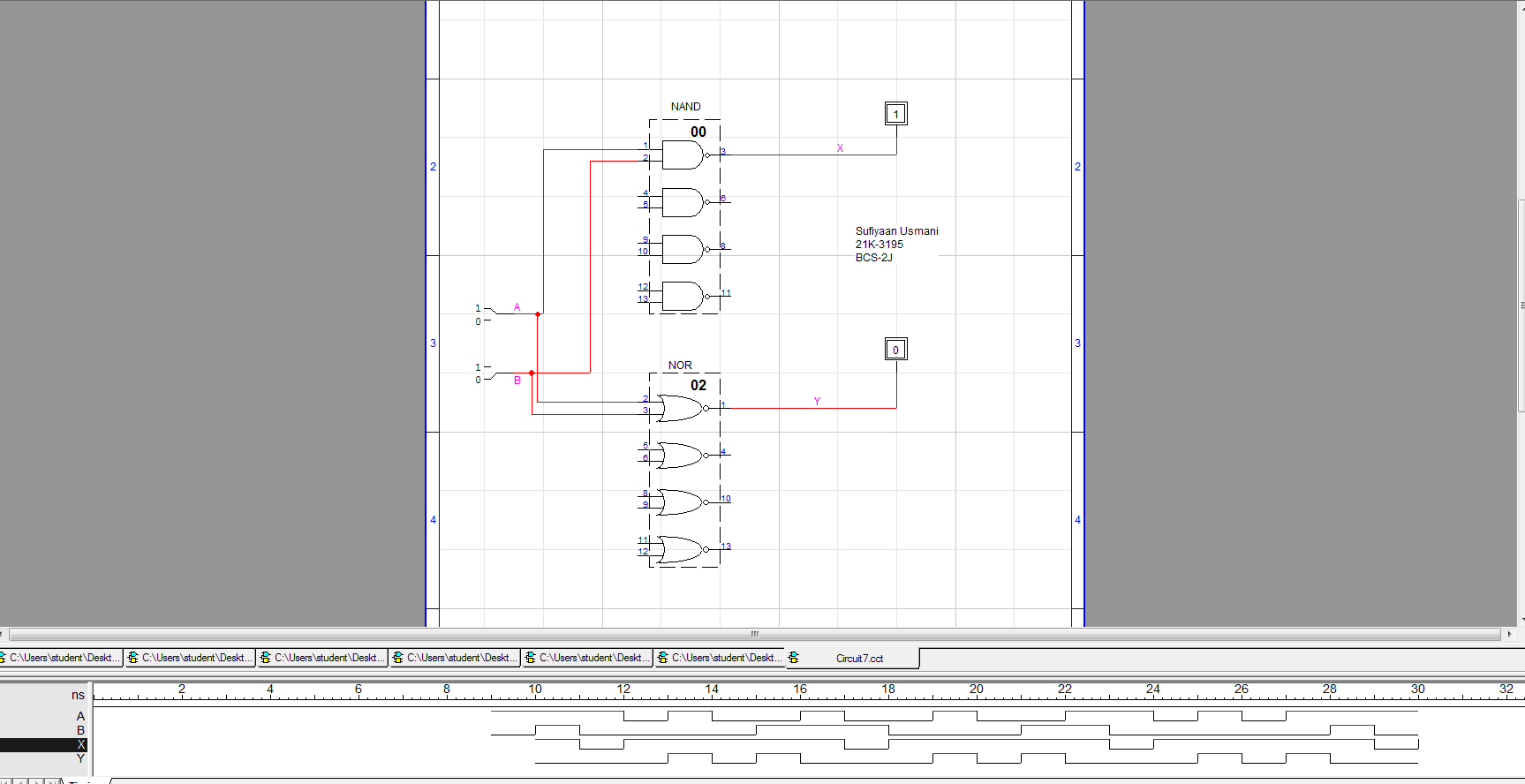
**Lab 03**

Exercise 1:



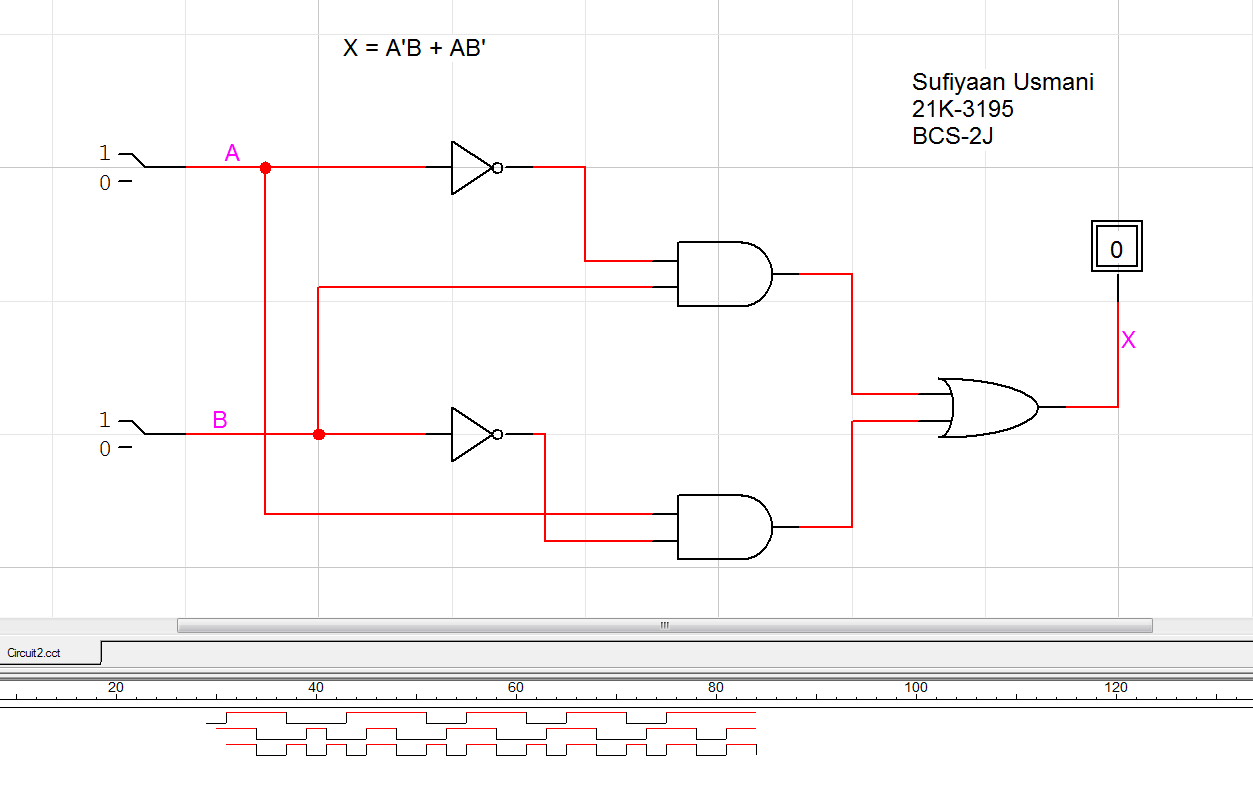
|  |  |  |  |
| --- | --- | --- | --- |
| A | B | X | Y |
| 0 | 0 | 1 | 1 |
| 0 | 1 | 1 | 0 |
| 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | 0 |

Exercise 2:



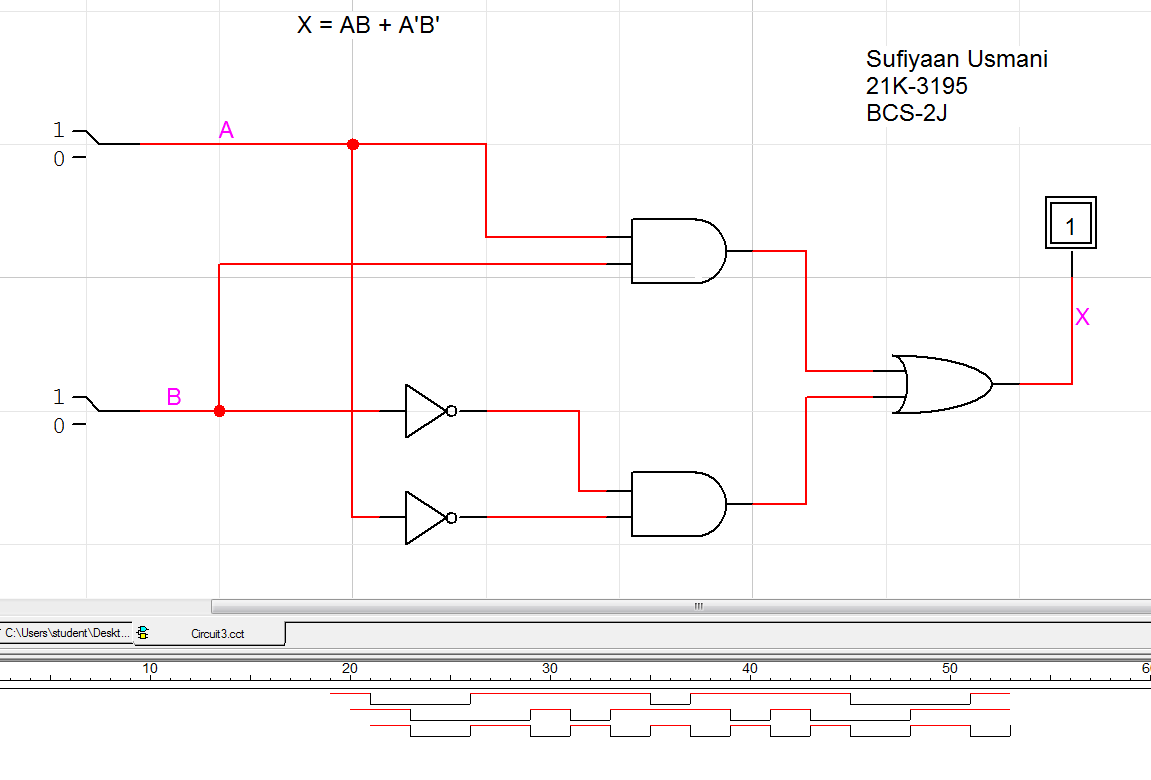
|  |  |  |  |
| --- | --- | --- | --- |
| A | B | X | Y |
| 0 | 0 | 1 | 1 |
| 0 | 1 | 1 | 0 |
| 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | 0 |

Exercise 3:



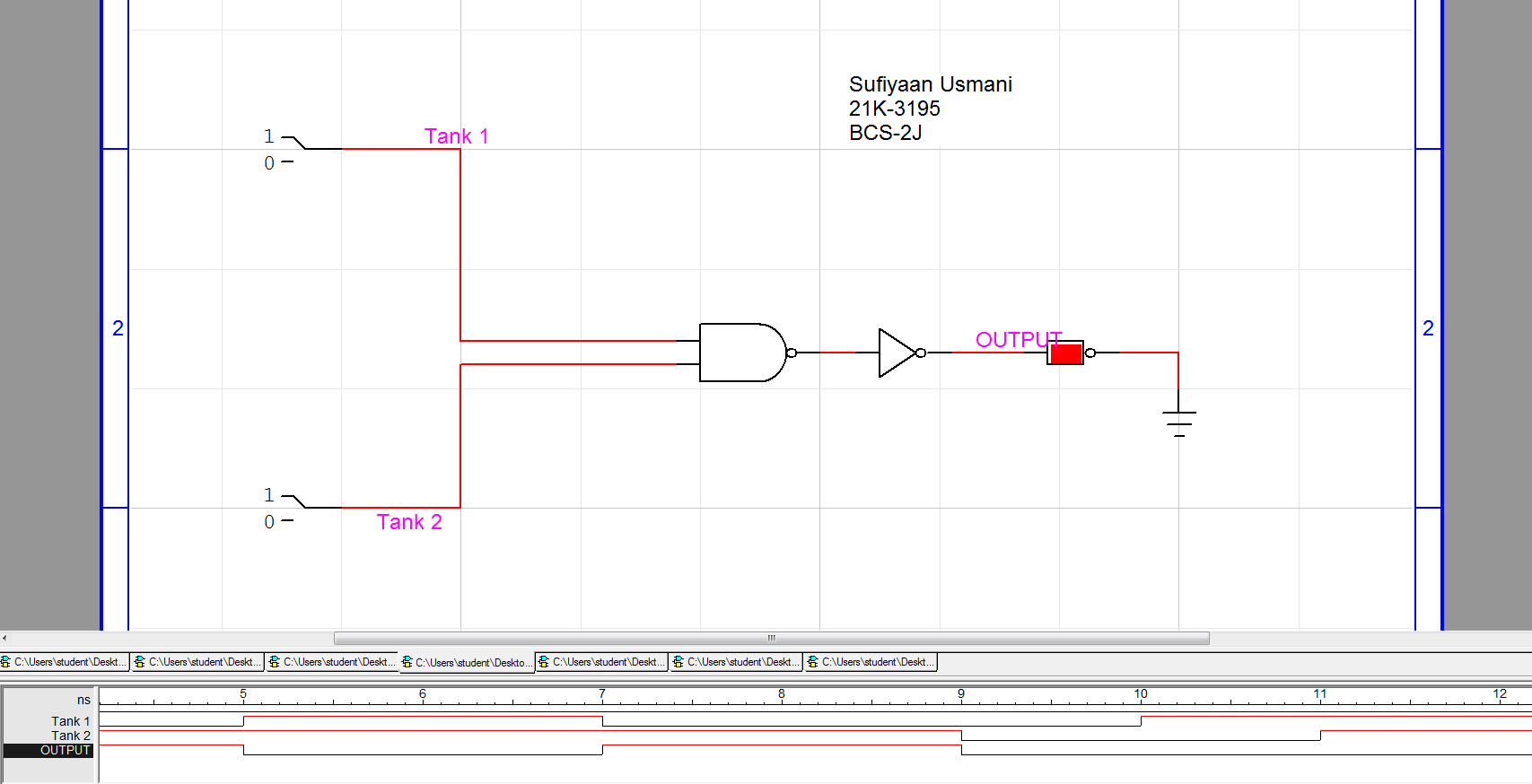
|  |  |  |
| --- | --- | --- |
| A | B | X |
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |

Exercise 4:



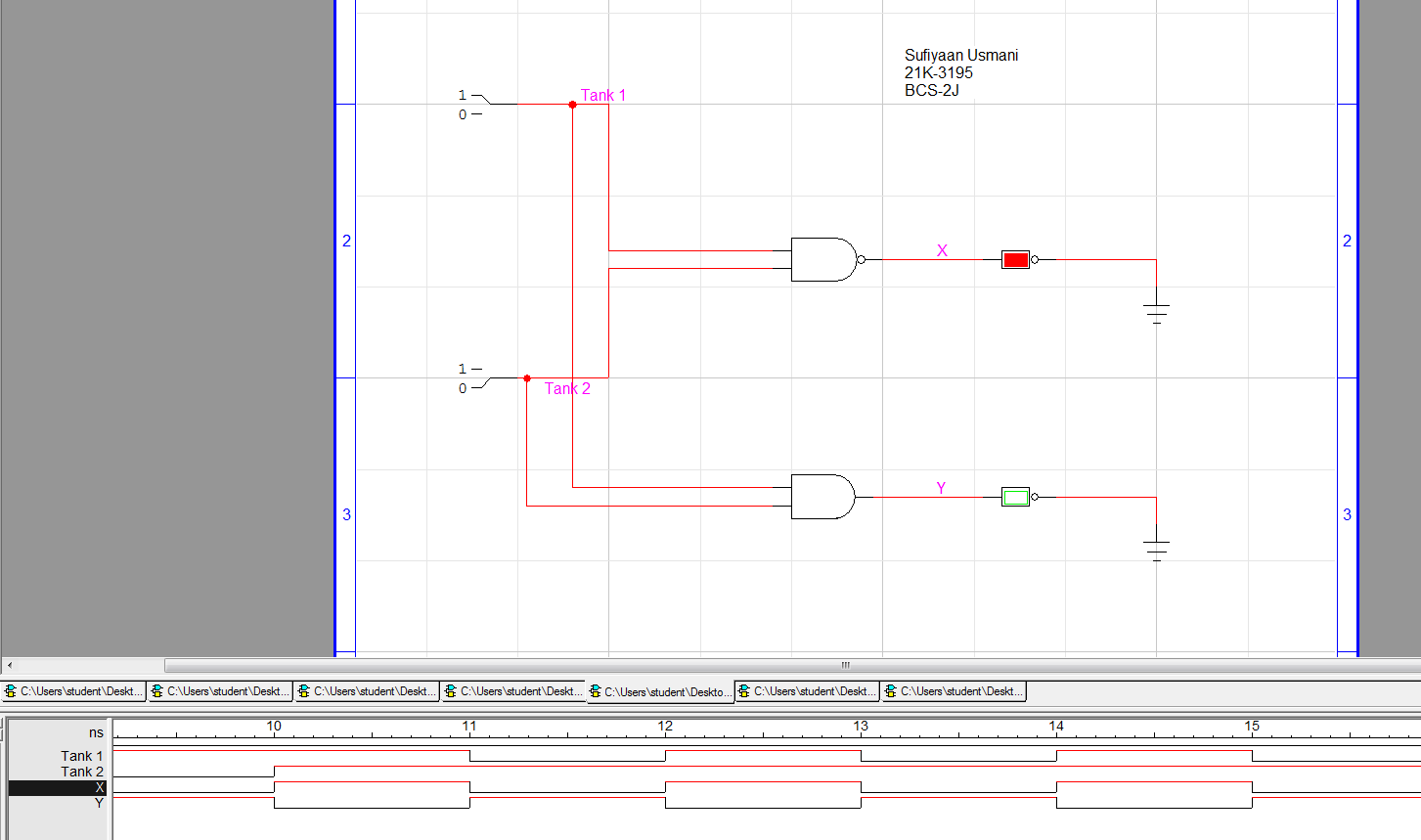
|  |  |  |
| --- | --- | --- |
| A | B | X |
| 0 | 0 | 1 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 1 |

Exercise 5:



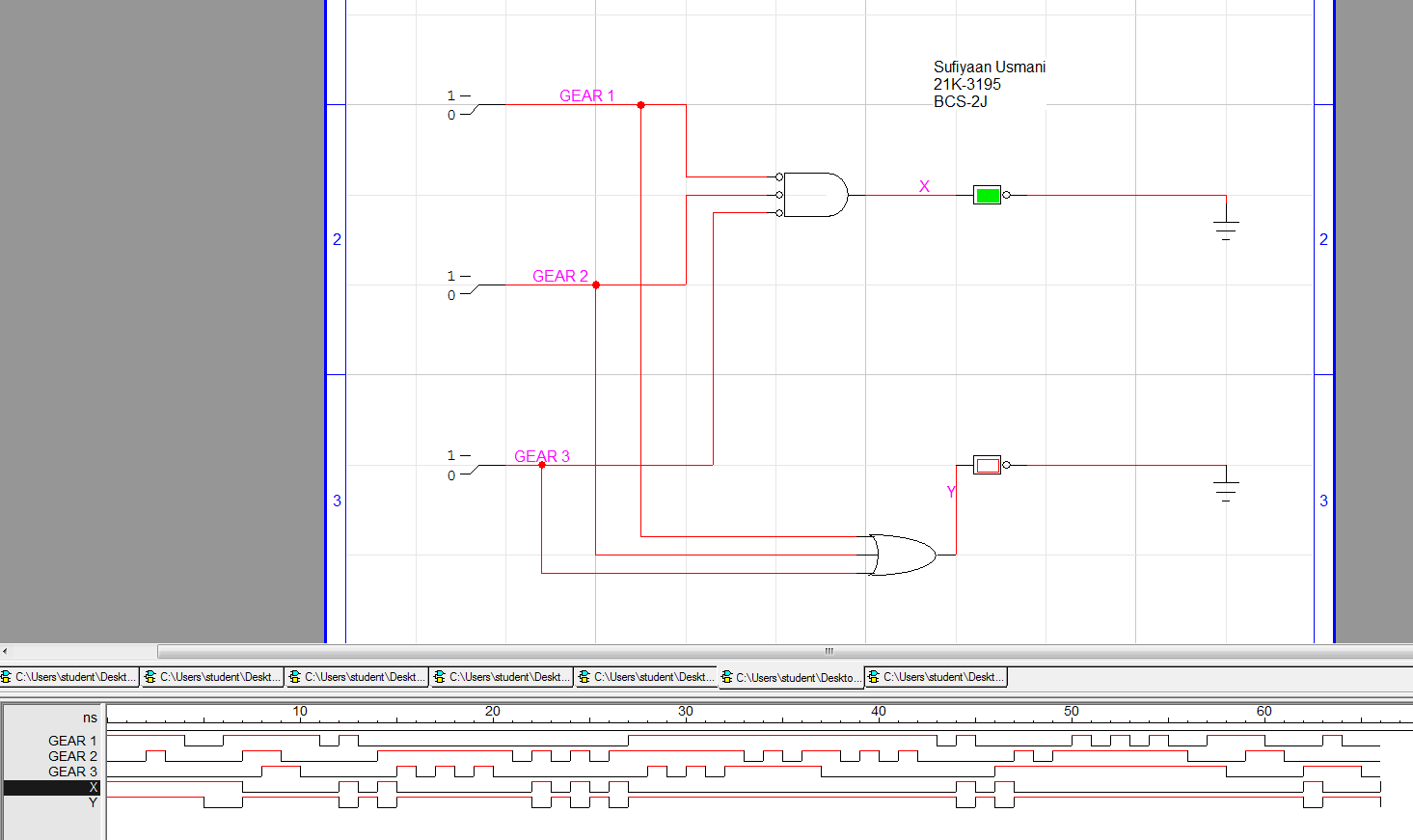
|  |  |  |
| --- | --- | --- |
| Tank 1 | Tank 2 | OUTPUT |
| 0 | 0 | 0 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 1 |

Exercise 6:



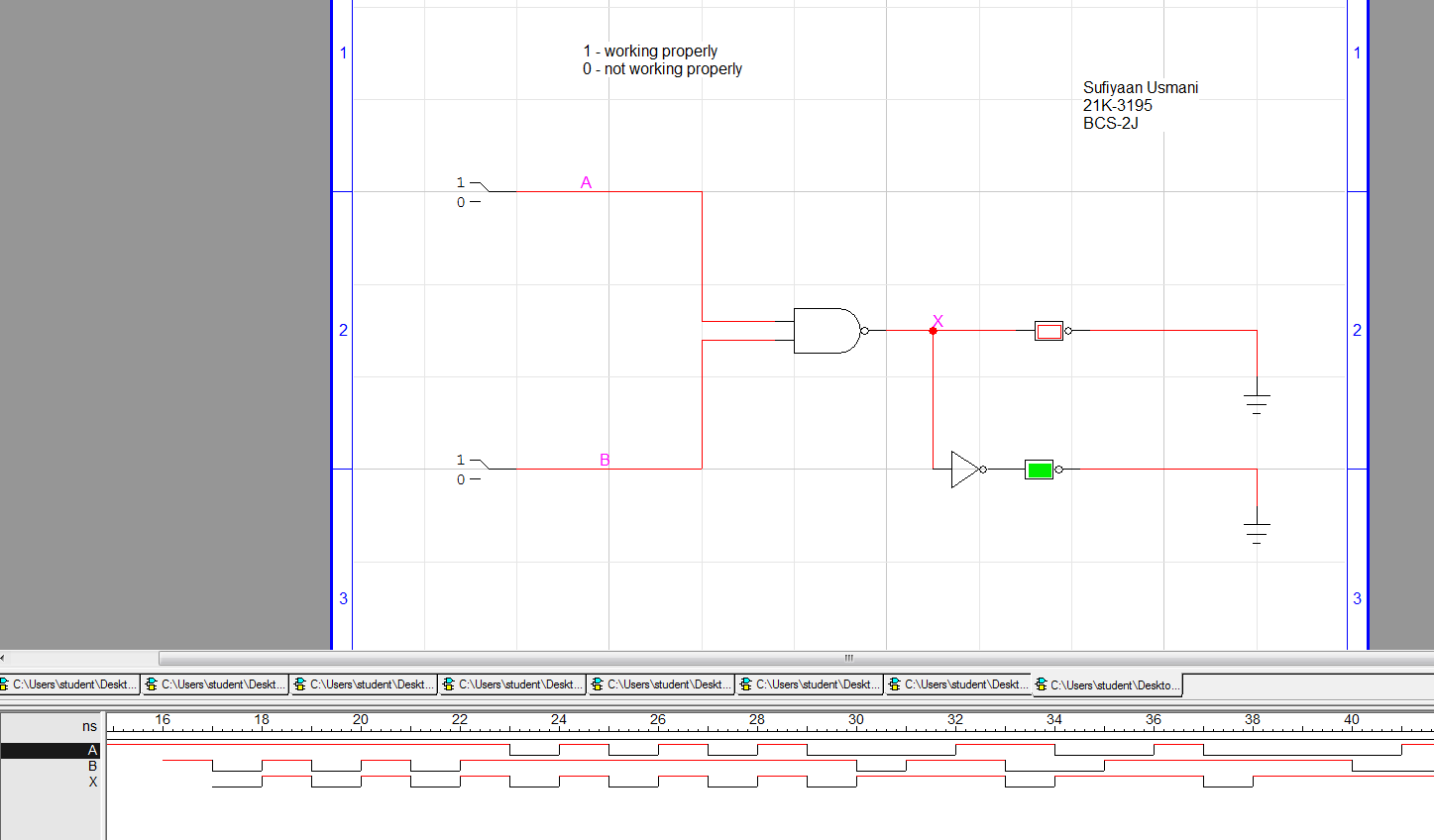
|  |  |  |  |
| --- | --- | --- | --- |
| Tank 1 | Tank 2 | X | Y |
| 0 | 0 | 1 | 0 |
| 0 | 1 | 1 | 0 |
| 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | 1 |

Exercise 7:



|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| GEAR 1 | GEAR 2 | GEAR 3 | X | Y |
| 0 | 0 | 0 | 1 | 0 |
| 0 | 1 | 0 | 0 | 1 |
| 1 | 0 | 1 | 0 | 1 |
| 1 | 1 | 0 | 0 | 1 |

Exercise 8:



Criteria:

0 – Working properly

1 – Not working properly

X - Error

|  |  |  |
| --- | --- | --- |
| A | B | X |
| 0 | 0 | 1 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |

TRUE/FALSE:

1. An inverter performs a NOT operation. **(True)**
2. A NOT gate cannot have more than one input. **(True)**
3. If any input to an OR gate is zero, the output is zero. **(False)**
4. If all inputs to an AND gate are 1, the output is 0. **(False)**
5. A NAND gate can be considered as an AND gate followed by a NOT gate. **(True)**
6. A NOR gate can be considered as an OR gate followed by an inverter. **(True)**
7. The output of an exclusive-OR is 0 if the inputs are opposite. **(False)**